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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/691,685	Confirmation No.: 6603
Applicant	:	Chi-Yang Lin et al.	
Title	:	DATA PROCESSING PATH SELECTION METHOD AND GRAPHICS PROCESSING SYSTEM UTILIZING THE SAME	
Filed	:	October 23, 2003	
TC/A.U.	:	2628	
Examiner	:	Hau H. Nguyen	
Docket No.	:	3304.2.96	
Customer No.	:	21552	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

A Final Office Action ("FOA") dated September 20, 2006 rejected all pending claims (claims 1-17) in the present application. A response to the FOA, which did not amend any of the claims, was submitted December 12, 2006. An Advisory Action Before the Filing of an Appeal Brief was mailed December 27, 2006 that refused to enter the previously-filed response. A timely Notice of Appeal was filed January 17, 2006. Appellants' Appeal Brief is filed herewith.

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REAL PARTY IN INTEREST

The real party in interest is the assignee, Via Technologies, Inc. of Taiwan, Republic of China.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and/or interferences.

STATUS OF CLAIMS

Claims 1-17 are pending in the present application. Claims 1-13 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,949,439 to Ben-Yoseph et al. (hereinafter, "Ben-Yoseph") in view of U.S. Patent Publication No. 2002/0194509 to Plante et al. (hereinafter, "Plante").

Claims 14, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ben-Yoseph in view of Plante, as applied to claim 1, and further in view of U.S. Patent No. 6,549,961 to Kloth (hereinafter, "Kloth").

Appellants appeal the rejection of claims 1-17.

STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection. In fact, no claim amendments have been filed during the prosecution of this case.

SUMMARY OF CLAIMED SUBJECT MATTER

As stated in the background section of Appellants' specification, present technology for displaying graphics (such as 3D graphics) on a screen is becoming increasing more difficult to use as the amount 3D graphics data ever increases with newer computer/video game systems. This

presently-known technology involves having an application program generate "vertex data" which is processed to obtain the corresponding coordinates (and shading requirements) that is projected onto the screen space. This vertex data involves performing transformation and lighting procedures, and may be implemented by a central processing unit (or "CPU") and a graphics processor that includes a transformation/lighting engine. However, in the prior art, either the CPU or the transformation/lighting engine, but not both, perform the desired operation.

With the increasing amount of graphics data associated with 3D images, machines using this technology may have trouble processing such data at the desired speed. Thus, it was an "object of the present invention to provide a data processing path selection method a graphics processing system utilizing such method so as to enhance processing speeds of 3D graphics data." Specification, pg. 2, paragraph [0005].

As required by 37 C.F.R. § 41.37(c)(1)(v), a summary of claimed subject matter immediately follows. The references to the specification refer only to embodiments of the invention. The invention is defined by the claims. Accordingly, these references to the specification are not meant to limit the scope of the claims at issue in any way but are only provided because they are mandated by 37 C.F.R. § 41.37(c)(1)(v). All references are to Appellants' specification and Figures are provided in parenthesis "( )" in the claims.

1. A data processing path selection method for use in a digital data processing system (Figure 3), said digital data processing system comprising a central processing unit (Figure 3 and pg. 5 paragraph [0026]) and a graphics processor (Figure 2b and pg. 5 paragraph [0026]), said graphics processor comprising a transformation/lighting engine (Figure 2b, Figure 3, and pg. 1 paragraph [0003]), said method comprising steps of:

receiving graphics data (Figure 3, pg. 2 paragraph [0006], and pg. 5 paragraph [0026]);

detecting a utilization rate of said central processing unit (Figure 3, pg. 2 paragraph [0006], and pg. 5 paragraph [0026]); and

allocating said graphics data to either said central processing unit or said transformation/lighting engine of said graphics processor according to said utilization rate of said central processing unit (Figure 3, pg. 2 paragraph [0006], and pg. 5 paragraph [0026]).

6. A data processing path selection method for use in a digital data processing system (Figure 3), said digital data processing system comprising a central processing unit (Figure 3 and pg. 5 paragraph [0026]), and a graphics processor (Figure 2b and pg. 5 paragraph [0026]), said graphics processor comprising a transformation/lighting engine (Figure 2b, Figure 3, and pg. 1 paragraph [0003]), said method comprising steps of:

receiving vertex data (Figure 3, pg. 3 paragraph [0011], and pg. 5 paragraph [0026]);

detecting a utilization rate of said central processing unit (Figure 3, pg. 3 paragraph [0011], pg. 5 paragraph [0026], and pg. 6 paragraph [0027]);

allocating said vertex data to said transformation/lighting engine of said graphics processor when said utilization rate of said central processing unit is greater than a first threshold value (Figure 3, pg. 3 paragraph [0011], pg. 5 paragraph [0026], and pg. 6 paragraph [0027]); and

allocating said vertex data to said central processing unit when said utilization rate of said central processing unit is less than a second threshold value (Figure 3, pg. 3 paragraph [0011], pg. 5 paragraph [0026], and pg. 6 paragraph [0027]).

11. A graphics processing system (Figure 3) comprising;

a central processing unit (Figure 3 and pg. 5 paragraph [0026]);

a graphics processor (Figure 2b) comprising a transformation/lighting engine, and receiving graphics data generated by an application program (Figure 2b, Figure 3, pg. 1 paragraph [0003], and pg. 5 paragraph [0026]); and

a path selection unit (Figure 3) electrically connected to said central processing unit and said transformation/lighting engine of said graphics processor (pg. 5 paragraph [0026]), and allocating said graphics data to either said central processing unit or transformation/lighting engine of said graphics processor according to a utilization rate of said central processing unit (pg. 5 paragraph [0026] and pg. 6 paragraph [0027]).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented for review:

Whether claims 1-13 and 17 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Ben-Yoseph and Plante.

Whether claims 14, 15, and 16 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Ben-Yoseph and Plante and further in view Kloth.

ARGUMENT

A. Claims 1-13 and 17 Rejected under 35 U.S.C. § 103(a)

1. All Claim Elements Are Not Taught

Claims 1-13 and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ben-Yoseph in view of Plante. This rejection is respectfully traversed.

The M.P.E.P. states that

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.
>
> The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.

M.P.E.P. § 2142.

Appellants respectfully submit that the claims at issue are patentably distinct from the

cited references. The cited references do not teach or suggest all of the limitations in these claims.

Independent claim 1 recites "detecting a utilization rate of said central processing unit" and then "allocating said graphics data to either said central processing unit or said transformation/lighting engine of said graphics processor according to said utilization rate of said central processing unit." As explained in the specification, this limitation means that the utilization rate of the central processing unit ("CPU") is detected to determine whether the CPU can help process graphics data. In other words, based upon this utilization rate of the CPU, some of the graphics data will be "allocat[ed] to the CPU instead of "the transformation/lighting engine of said graphics processor," thereby increasing the overall speeds in processing the graphics data.

Such a claim limitation regarding allocating the graphics data to the CPU based upon the utilization rate of the CPU is not taught or suggested by Ben-Yoseph or Plante. In the FOA, the Examiner acknowledges that such a claim limitation is not taught or suggested by Ben-Yoseph. Such a limitation is also absent from the Plante reference. As acknowledged by the Examiner, Plante discloses calculating the CPU utilization rate for the purpose of making a CPU performance level assessment. The purpose of this performance assessment is to determine whether less power can be used by the CPU. For example, if prior CPU utilization and/or policies dictate a different CPU performance level, the CPU performance level is changed (See Plante's Abstract). More concretely, if the CPU utilization determination indicates that less CPU processing speed could adequately fulfill processing needs, the CPU is instructed to *decrease processing speed* to consume less power (pg 1, paragraph [0004]). Accordingly, Plante detects the utilization rate of the CPU in order to opportunely change the performance level of the CPU. There is no teaching or suggestion in Plante that the utilization rate of CPU is detected to see if it can help *other devices for additional work*. In other words, there is no teaching or suggestion that the utilization rate is detected and then the graphics data is "allocate[d]" to the CPU or the "transformation/lighting engine of said graphics processor *according to said utilization rate of said central processing unit*." As such, this claim limitation is not taught or suggested by the cited references and claim 1 cannot be rejected under § 103(a). Withdrawal of this rejection is respectfully requested.

Claims 2-5 depend directly from claim 1. Accordingly, Appellants respectfully request that the rejection of claims 2-5 be withdrawn for at least the same reasons as those presented above in connection with claim 1.

With respect to independent claim 6, this claim includes language that requires "detecting a utilization rate of said central processing unit" and then "allocating said vertex data to said transformation/lighting engine of said graphics processor when said utilization rate of said central processing unit is greater than a first threshold value" and "allocating said vertex data to said central processing unit when said utilization rate of said central processing unit is less than a second threshold value." Again, such limitations are not taught or suggested by the cited references. Specifically, the Examiner acknowledges that such claim limitations are not taught or suggested by Ben-Yoseph. Moreover, with respect to Plante, this reference teaches detecting the CPU utilization rate for purposes of reducing processing speeds, when necessary, as a means of optimizing power consumption. This reference clearly does *not* teach allocating vertex data (or graphics data) to the CPU or to a transformation/lighting engine based upon the CPU utilization rate, as is required by claim 6. As such, because all of the claim limitations of claim 6 are not taught or suggested by the cited references, this claim cannot be rejected under § 103(a). Withdrawal of this rejection is respectfully requested.

Claims 7-10 depend directly from claim 6. Accordingly, Appellants respectfully request that the rejection of claims 7-10 be withdrawn for at least the same reasons as those presented above in connection with claim 6.

With respect to independent claim 11, this claim recites "a path selection unit electrically connected to said central processing unit and said transformation/lighting engine of said graphics processor, and allocating said graphics data to either said central processing unit or transformation/lighting engine of said graphics processor according to a utilization rate of said central processing unit." Again, the claim limitation regarding "allocating" the graphics data to the CPU or the transformation/lighting engine "according to a utilization rate of said central processing unit" is not taught by Ben-Yoseph. At best, Plante teaches using the CPU utilization rate for purposes of reducing processing speeds, when necessary, as a means of optimizing power consumption, which is clearly not the same as allocating graphics data based upon the CPU utilization rate. As such, because all of the claim limitations of claim 11 are not taught or

suggested by the cited references, this claim cannot be rejected under § 103(a). Withdrawal of this rejection is respectfully requested.

Claims 12-13 and 17 depend directly from claim 1. Accordingly, Appellants respectfully request that the rejection of claims 12-13 and 17 be withdrawn for at least the same reasons as those presented above in connection with claim 11.

2. A Combination of the Cited References Does Not Result In the Claimed Invention

Moreover, with respect to claims 1-13 and 17, the Applicants further assert that the present rejection is improper because, even if Ben-Yoseph and Plante were combined in the manner asserted by the Examiner, the resulting combination would still not arrive at the claimed invention. As acknowledged by the Examiner, Ben-Yoseph teaches a system in which the host processor 102 and the multimedia processor 106 operate in concert to balance the execution load between the host processor 102 and multimedia processor 106. Plante teaches calculating the CPU utilization rate for the purpose of a CPU performance level assessment. As a matter of fact, these two functions do not conflict with each other and can be co-existent in a computer system. Therefore, combining Ben-Yoseph with Plante, in the manner asserted, would result in a computer system exhibiting both of these functions, *i.e.*, a system in which the resource manager shifts complex graphics operations to the DIB engine driver on the host processor if the multimedia processor is overloaded (such as taught by Ben-Yoseph) and a system in which the CPU performance level is changed when the CPU utilization and/or policies dictate a different CPU performance level (as taught by Plante). However, this combined system would still not allocate graphics data or vertex data to the CPU based upon the utilization rate of the CPU, as is required by claims 1-13 and 17. (Again, this requirement of the present claims is described in greater detail above). Thus, even if Ben-Yoseph and Plante were combined in the manner asserted, the resulting combination would not produce the claimed invention that allocates the vertex data or graphics data according to the CPU utilization rate. As such, a rejection under § 103(a) is improper and must be withdrawn.

3. There Is No Motivation to Combine Ben-Yoseph With Plante

Further, the Applicants submit herein that there is no teaching or motivation that would have led a skilled artisan to combine Ben-Yoseph with Plante. Plante discloses calculating CPU utilization rate for the purpose of CPU performance level assessment. This means that the utilization rate is monitored to optimize power consumption. According to Ben-Yoseph, whether the CPU can help in processing graphics data *does not* depend on the utilization rate of the CPU, but instead depends on the burden of the multimedia processor. Under this circumstance, it does not matter whether the CPU utilization rate is detected or not. In other words, Ben-Yoseph's system balances the execution load between the host processor 102 and the multimedia processor 106 (Ben-Yoseph col. 7, lines 20-35), regardless of whether the utilization rate is detected. Furthermore, according to Ben-Yoseph, the resource manager 308 shifts complex graphics operations to the DIB engine drive on the host processor 102 in the case that the multimedia processor 106 is overloaded, so it is not necessary to detect the CPU utilization rate.

Because Ben-Yoseph's system operates independent of the CPU utilization rate, there is no indication why one skilled in the art would be concerned about Ben-Yoseph's utilization rate, nor is there is any indication or motivation why one skilled in the art would have combined Ben-Yoseph's system with the teachings of CPU utilization rate detection in Plante. Accordingly, the rejection based upon § 103(a) is improper.

Accordingly, based upon the foregoing reasons, the rejection of claims 1-13 and 17 under § 103(a) is improper. Withdrawal of this rejection is respectfully requested.

B. Claims 14, 15, and 16 Rejected under 35 U.S.C. § 103(a)

Claims 14, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ben-Yoseph in view of Plante and in further view of Kloth. This rejection is respectfully traversed. The standard for establishing a *prima facie* case of obviousness is provided above.

Appellants respectfully submit that the claims at issue are patentably distinct from the cited references. The cited references do not teach or suggest all of the limitations in these claims.

Claims 14, 15, and 16 depend either directly from claim 11. Accordingly, Appellants respectfully request that the rejection of claims 14, 15, and 16 be withdrawn for at least the same reasons as those presented above in connection with claim 11. The addition of Kloth does nothing to overcome the deficiencies of Ben-Yoseph and Plante discussed above. Specifically, Applicants can find no teaching or disclosure in Kloth of "a path selection unit" that "allocate[s]" graphics data to the "central processing unit and ...[the] transformation/lighting engine... according to a utilization rate of said central processing unit." In fact, Applicants cannot find any disclosure in Kloth regarding the use of the CPU utilization rate to allocate graphics data. Accordingly, because Kloth, Ben-Yoseph, or Plante fail to teach all of the claimed limitations of claims 14, 15, and 16, these claims cannot be rejected under § 103(a). Withdrawal of this rejection is respectfully requested.

Respectfully submitted,

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CLAIMS APPENDIX

Listing of Claims involved in the appeal:

1. A data processing path selection method for use in a digital data processing system, said digital data processing system comprising a central processing unit and a graphics processor, said graphics processor comprising a transformation/lighting engine, said method comprising steps of:

receiving graphics data;

detecting a utilization rate of said central processing unit; and

allocating said graphics data to either said central processing unit or said transformation/lighting engine of said graphics processor according to said utilization rate of said central processing unit.

2. The data processing path selection method according to claim 1 wherein said graphics data are vertex data generated by an application program.

3. The data processing path selection method according to claim 1 wherein said step of detecting said utilization rate of said central processing unit is performed by periodically sampling command flows of said central processing unit.

4. The data processing path selection method according to claim 1 wherein said step of allocating said graphics data to either said central processing unit or said transformation/lighting engine of said graphics processor is performed by the following sub-steps:

allocating said graphics data to said transformation/lighting engine of said graphics processor when said utilization rate of said central processing unit is equal to or greater than a threshold value; and

allocating said graphics data to said central processing unit when said utilization rate of said central processing unit is less than said threshold value.

5. The data processing path selection method according to claim 1 wherein said digital data processing system is a computer system.

6. A data processing path selection method for use in a digital data processing system, said digital data processing system comprising a central processing unit and a graphics processor, said graphics processor comprising a transformation/lighting engine, said method comprising steps of:

receiving vertex data;

detecting a utilization rate of said central processing unit;

allocating said vertex data to said transformation/lighting engine of said graphics processor when said utilization rate of said central processing unit is greater than a first threshold value; and

allocating said vertex data to said central processing unit when said utilization rate of said central processing unit is less than a second threshold value.

7. The data processing path selection method according to claim 6 wherein said vertex data are generated by an application program.

8. The data processing path selection method according to claim 6 wherein said first threshold value is identical to said second threshold value.

9. The data processing path selection method according to claim 6 wherein said step of detecting said utilization rate of said central processing unit is performed by periodically sampling command flows of said central processing unit.

10. The data processing path selection method according to claim 6 wherein said digital data processing system is a computer system.

11. A graphics processing system comprising;

a central processing unit;

a graphics processor comprising a transformation/lighting engine, and receiving graphics data generated by an application program; and

a path selection unit electrically connected to said central processing unit and said transformation/lighting engine of said graphics processor, and allocating said graphics data to either said central processing unit or transformation/lighting engine of said graphics processor according to a utilization rate of said central processing unit.

12. The graphics processing system according to claim 11 wherein said path selection unit periodically samples command flows of said central processing unit to realize said utilization rate of said central processing unit.

13. The graphics processing system according to claim 11 wherein said path selection unit allocates said graphics data to said transformation/lighting engine of said graphics processor when said utilization rate of said central processing unit is equal to or greater than a threshold value, and allocates said graphics data to said central processing unit when said utilization rate of said central processing unit is less than said threshold value.

14. The graphics processing system according to claim 11 wherein said path selection unit is incorporated in a north bridge chip.

15. The graphics processing system according to claim 11 wherein said path selection unit is implemented by hardware.

16. The graphics processing system according to claim 11 wherein said path selection unit is implemented by firmware.

17. The graphics processing system according to claim 11 wherein said graphics data are vertex data.

EVIDENCE APPENDIX

NONE.

RELATED PROCEEDINGS APPENDIX

NONE.